AMENDMENTS TO THE CLAIMS:

Claim 1. (Previously presented) A method for fabricating a semiconductor device comprising, in consecutive order:

depositing a metallic conductive film on an underlying insulating film;

consecutively depositing first and second insulator films on said metallic conductive film;

patterning said first and second insulator films to have a substantially same patterned area;

etching said second insulator film selectively from said first insulator film to configure said second insulator film to have a bottom with a width smaller than a width of said first insulator film;

patterning said metallic conductive film by using said first and second insulator films as an etching mask;

subsequently depositing a third insulator film on said first insulator film, said etched second insulator film, and said underlying insulating film;

etching-back said third insulator film to configure a side-wall film covering at least said patterned metallic conductive film; and

depositing a fourth insulator film to embed therein said side-wall film on said underlying insulating film.

Claim 2. (Previously presented) The method according to claim 1, wherein said etching-back configures said side-wall film to have a tapered mesa structure having a larger width toward a bottom thereof.

Claim 3. (Previously presented) The method according to claim 1, further comprising, after depositing said fourth insulator film:

etching said fourth insulator film to form therein a contact hole by using said side-wall film as an etch stopper; and

forming a contact plug in said contact hole.

Claim 4. (Previously presented) The method according to claim 1, wherein said first and second insulator films comprise a nitride film and an oxide film, respectively.

Claim 5. (Previously presented) The method according to claim 1, wherein said semiconductor device comprises a semiconductor memory device.

Claim 6. (Previously presented) A method for fabricating a semiconductor device comprising, in consecutive order:

depositing a metallic conductive film on an underlying insulating film;

consecutively depositing first and second insulator films on said metallic conductive film;

patterning said first and second insulator films to have a substantially same patterned area;

patterning said metallic conductive film by using said first and second insulator films as an etching mask;

etching said second insulator film selectively from said first insulator film to configure said second insulator film to have a bottom with a width smaller than a width of

said first insulator film;

subsequently depositing a third insulator film on said first insulator film, said etched second insulator film, and said underlying insulating film;

etching-back said third insulator film to configure a side-wall film covering at least said patterned metallic conductive film; and

depositing a fourth insulator film to embed therein said side-wall film on said underlying insulating film.

Claim 7. (Previously presented) The method according to claim 6, wherein said etching-back configures said side-wall film to have a tapered mesa structure having a larger width toward a bottom thereof.

Claim 8. (Previously presented) The method according to claim 6, further comprising, after depositing said fourth insulator film:

etching said fourth insulator film to form therein a contact hole by using said side-wall film as an etch stopper; and

forming a contact plug in said contact hole.

Claim 9. (Previously presented) The method according to claim 6, wherein said first and second insulator films comprise a nitride film and an oxide film, respectively.

Claim 10. (Previously presented) The method according to claim 6, wherein said semiconductor device comprises a semiconductor memory device.

Claim 11. (Currently amended) A method for fabricating a semiconductor device, the method comprising:

depositing a metallic conductive film on an insulating film;

depositing a first insulator film on said metallic conductive film;

depositing a second insulator film on said first insulator film;

patterning said first and second insulator films;

etching said second insulator film to have a patterned area that is ~~bottom with a width~~ smaller than ~~a width of the bottom of~~ said first insulator film;

patterning said metallic conductive film; ~~and~~

subsequently depositing a third insulator film on said first insulator film, said etched second insulator film, and said insulating film; and

forming a sidewall film by etching said third insulator film.

Claim 12. (Canceled).

Claim 13. (Currently amended) The method of claim 11, wherein said etching of said second insulator film is performed before said patterning of said metallic conductive film.

Claim 14. (Currently amended) The method of claim 11, wherein said etching of said second insulator film is performed after said patterning of said metallic conductive film.

Claim 15. (Previously presented) The method of claim 11, wherein said patterning said metallic conductive film uses said first and second insulator films as an etching mask.

Claims 16-17. (Canceled).

Claim 18. (Currently amended) The method of claim 11 ~~17~~, wherein said sidewall film covers at least said patterned metallic conductive film.

Claim 19. (Previously presented) The method of claim 18, further comprising depositing a fourth insulator film on said sidewall film and said underlying insulating film.

Claim 20. (Previously presented) The method of claim 19, further comprising etching said fourth insulator film to form a contact hole.

Claim 21. (Previously presented) The method of claim 20, wherein etching said fourth insulator film uses said sidewall film as an etch stopper.

Claim 22. (Previously presented) The method of claim 20, further comprising forming a contact plug in said contact hole.

Claim 23. (Currently amended) The method of claim 11 ~~17~~, wherein said sidewall film comprises a tapered mesa structure having a width larger at the bottom.

Claim 24. (Previously presented) The method of claim 11, wherein said first insulator film comprises a nitride film.

Claim 25. (Previously presented) The method of claim 11, wherein said second insulator film comprises an oxide film.

Claim 26. (Previously presented) The method of claim 11, wherein said semiconductor device comprises a semiconductor memory device.

Claim 27. (Previously presented) The method of claim 1, wherein etching said second insulator film selectively from said first insulator film comprises wet etching said second insulator film.

Claim 28. (Previously presented) The method of claim 6, wherein etching said second insulator film selectively from said first insulator film comprises wet etching said second insulator film.

Claim 29. (Previously presented) The method of claim 11, wherein etching said second insulator film comprises wet etching said second insulator film.